

Docket No.: L&L-I0232

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By: 

Date: April 1, 2002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Wolfgang Rösner et al.  
Applic. No. : 10/047,013  
Filed : January 16, 2002  
Title : Method for Producing a Vertical Semiconductor Transistor  
Component and Vertical Semiconductor Transistor Component  
Art Unit : 2811

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner of Patents and Trademarks,  
Washington, D.C. 20231

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

United States Patent No. 5,714,766 (Chen et al.), dated February 3, 1998;

German Patent DE 196 32 835 C1 (Schäfer et al.), dated April 2, 1998, method for producing a capacitor in a semiconductor configuration;

European Patent Application EP 0 843 361 A1 (Nakazato et al.), dated May 20, 1998;

H.I. Liu et al.: "Self-limiting oxidation for fabricating sub-5 nm silicon nanowires", Appl. Phys. Lett., Vol. 64, No. 11, March 14, 1994, pp. 1383-1385;

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Harald Gossner et al.: "Vertical Si-Metal-Oxide-Semiconductor Field Effect Transistors with Channel Lengths of 50 nm by Molecular Beam Epitaxy", Jpn. J. Appl. Phys., Vol. 33, 1994, pp. 2423-2428;

Lothar Risch et al.: "Vertical MOS Transistors with 70 nm Channel Length", IEEE Transactions on Electron Devices, Vol. 43, No. 9, September 1996, pp. 1495-1498;

Hiroshi Fukuda et al.: "Fabrication of silicon nanopillars containing polycrystalline silicon/insulator multilayer structures", Appl. Phys. Lett., Vol. 70, No. 3, January 20, 1997, pp. 333-335;

Hiroshi Mizuta et al.: "High-speed single-electron memory: cell design and architecture", XP-002151823, IEEE 1998, pp. 67-72.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the applicant.

Respectfully submitted,

  
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For Applicants

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Date: April 1, 2002

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